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Power Efficient Design of BILBO using Various Sequential Elements for Low power VLSI Applications (Basic 5T-transistor and 5T- with MTCMOS)

P.Nagarajan[*1], K.Nithya[2]

[*1]Assistant Professor, ECE, PSNA College of Engg &Tech, Dindigul, Tamilnadu, India

[2] Assistant Professor, ECE, Theni Kammavar Sangam College of Technology, Theni,Tamil Nadu, India

nagarajan.research@gmail.com

Abstract

This paper enumerates low power design of BILBO(Built-In- Logic-Block-Observer) using Basic 5T-TSPC clocked latch and 5T-TSPC(MTCMOS) clocked latch.The clocked latches are basic building block to design the BILBO.The clocked latches consumes more power in the total power consumption of the BILBO.The power efficient 5T-TSPC(MTCMOS) clocked latch is designed from the Basic 5T-TSPC clocked latch. The BILBO is designed by using both Basic 5T-TSPC clocked latch and 5T-TSPC(MTCMOS) clocked latch.The design of BILBO by using 5T-TSPC(MTCMOS) consumes less power.The performance of BILBO is analyzed in terms of NumberofTransistors(NT),NumberOfClockedTransistors(NC),Power(P),Area(A).

Keywords : Clocked Latch (Flip-flop), BILBO, Low power, Area.

Introduction

Clocked Latch

The combination of combinational circuit and memory element is called sequential circuit.Latch or Flip-flop is a memory element in sequential circuit.In a sequential circuit the memory element is required to know what has happened in the past. Flip-flop(Clocked latch)[5] and latch is a circuit that has two stable states and can be used to store state information.The latch with the additional control input is called Clocked latch(Flip-flop).The additional control input is called clock.The clock provides the time reference point determine the movement of data in a digital system.The clocked latch[5] is a basic building block to design any clocking system.The clocking system consists of a clock distribution network and clocked latch.The designed of clocked latch is crucial for the design of low power circuits as a digital block contains many memory elements.[1].A large portion of the on chip power is consumed by the clocking system.The total power consumption of the clocking system depends on both clock distribution network and clocked latches(Flip-flops)[6].The power consumption of clocked latch is higher than that of the clocking distribution network.The clocked latch is defined as “leading edge triggered”. When the transition of the clock from 0-to-1,the output (Q) is produced the same value of input(D).Conversely in a “negative edge triggered clocked latch”.It is also possible to build a “double-edge triggered clocked latch”,that responds to both leading edge and trailing edge of the clock ‘C’.

BILBO

BIlBO(Built-In-Logic-Block-Observer)is one of the BIST architecture.

BIST

BIST stands for Built-In-Self-Test. A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test(BIST)[7]capability inside the chip.This increases the controllability and observability of the chip.Controllability is the ability to set(to1) and reset(to 0) every node internal to the circuit.Observability is the ability to observe either directly or indirectly the state of any node in the circuit.This makes the test generation and fault detection is easy.In BIST, the test generation[3] and the output response evaluation are done in chip.A basic BIST configuration is shown in Fig 1.

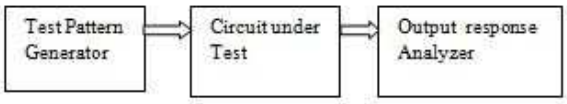

Fig 1:BIST configuration

The main function of the test pattern generator is to apply test patterns to the unit under test.The resulting output pattern are transferred to the output response analyzer.A BIST scheme should be easy to important and must provide a high fault coverage. BILBO has become one of the most widely technique for self-testing of complex digital

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IC's.This technique is based on grouping the storage elements of the circuit,the method of incorporating a Built-In-Self-Test module is to use signature analysis or cyclic redundancy checking.A signature analyzer is constructed by cyclically adding the outputs of a circuit to the shift register if successive logic blocks are to be tested.Signature analysis can be merged with the scan technique to create a structure know as BILBO for Built-In-Logic Block Observation.It uses multipurpose module,called BILBO[3],that can be configured as function as an input test pattern generator or an output signature analyzer.This is composed of a row of clocked latches and feed back operation[7].Fig 2 shows logic diagram of a BILBO.The two control inputs B1 and B2 are used to select one of the four function modes.

1. Mode 1:B1=0, B2=1, All clocked latches are reset.

2.**Mode2:**B1=1,B2=1, The BILBO behaves are latch.The input x1,x2,x3 can be simultaneously clocked into the clocked latches and can be read from the Q and output.

3.Mode 3: B1=0,B2=0 the BILBO act as a serial SR.Data are serially clocked into the register through Sin,while the register contents can be simultaneously read at the parallel Q and Q outputs or clocked out through the Sout.

4. Mode 4:B1=1, B2=0, The BILBO is converted into a MISR.In this mode, it may used for performing parallel signature analysis or for generating pseudorandom sequences.

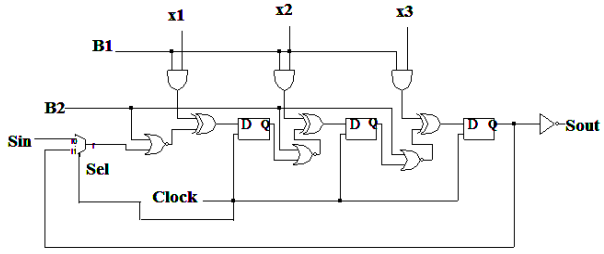

Fig 2: Logic diagram of a BILBO

Section II describes the clocked latches Basic 5T-TSPC and 5T-TSPC (MTCMOS).Section III explains the proposed BILBO by using 5T-TSPC clocked latch and BILBO by using 5T-TSPC (MTCMOS) clocked latch. Section IV discusses the simulation results of clocked latches and BILBO. Section V gives conclusions.

Clocked Latch

Basic 5T-TSPC clocked latch

TSPC (True Single Phase Clock) [10] circuit technique uses only a single clock and two to three clocked transistors. [1] In each latch without local inversion of the clock. An inversion of clock requires more clocked devices. The schematic of Basic 5T-TSPC clocked latch is shown in Fig 3.

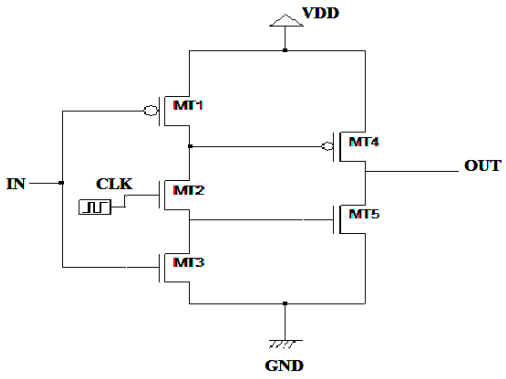

Fig 3: Schematic of 5T-TSPC Clocked Latch

This Basic 5T-TSPC clocked latch consists of only 5 transistors such as MT1, MT2, MT3,MT4 and MT5.The MT2 transistor is clocked transistor. The less number of transistors in clocked latch is used to reduce total power consumption of the circuit. This clocked latch is positive edge triggered clocked latch. This TSPC-Split-Output latch [1] is used to reduce threshold voltages. [3].In this latch the output of first stage is split. The clocked transistor is less in this latch, so the power spent on the clocked node is also minimized. It has 3NMOS transistors and 2 PMOS transistors. It is a D clocked latch.D clocked latch is an opaque storage element there is no relationship between the output and present values of the input.

When clock is high, the input is low, MT1, MT2, MT4 transistors are ON.MT3, MT5 transistors are OFF, so the output becomes high. When the clock is high and input is high, MT2,MT3,MT4 are ON,MT1 and MT5 transistors are OFF, then the output becomes zero.

When clock is low and also the input is low, MT1 transistor is only ON, MT2, MT3, MT4, MT5 are OFF, and then the output becomes zero. When the clock is low and input is high, then the output becomes zero.

This clocked latch performance is analyzed in terms of Number of Transistors (NT), Number of Clocked Transistors (NC), Power (P) and Area (A).The clocked latch is designed with various VLSI technologies like 0.12µm, 0.18 µm and various supply voltages (VDD) are 1.2v, 1.8v.This performance is shown in Table 1,2,3,4.

5T-TSPC (MTCMOS) clocked latch

5T-TSPC (MTCMOS) clocked latch is designed from Basic 5T-TSPC clocked latch. It is used to reduce the power consumption.

2.2.1 MTCMOS

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Multi threshold CMOS (MTCMOS) is a variation of CMOS chip technology [8].The MTCMOS is implemented by use of sleep transistors for reducing power. Logic is supplied by virtual power rail. Low Vth devices are used in the logic where fast switching, speed is important. High Vth devices connecting the power rails are turned ON in active mode, OFF in sleep mode. High Vth devices are as sleep transistors to reduce the static leakage power. The multi threshold voltage (MTCMOS) [2] circuit was proposed by inserting high threshold devices in series into low –Vth circuitry. The schematic of 5T-TSPC (MTCMOS) clocked latch is shown in Fig 4.A sleep control scheme is introduced for efficient power management. This technique inserts an extra series-connected transistor in the pull-down/pull-up path of a gate and turns it"off'"in the standby mode of operation. During regular mode of operation, the extra transistor is turned on. This provides substantial savings in leakage current during standby mode of operation. [1].

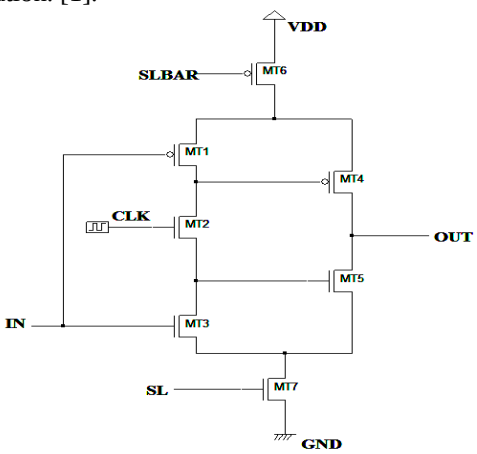

Fig 4: Schematic of 5T-TSPC (MTCMOS)

When clock is high, input is low, SL is low, MT1, MT2, MT5, MT6 transistors are ON, MT3, MT4, MT7 are turned OFF, and so the output becomes zero. When clock is high, input is low SL is high, then the output becomes zero. When clock is high, input is high, SLis low, MT1, MT5, MT7transistors are OFF, MT2, MT3, MT4, MT6 are ON, and so the output becomes high. When clock is high, input is high SL is high, then the output becomes zero.

This clocked latch performance is described in terms of Number Of Transistors(NT),Number Of Clocked Transistors(NC),Power(P),Area(A). The clocked latch is applied with various VLSI technologies like 0.12 µm, 0.18 µm and various supply voltages (VDD) are 1.2v, 1.8v.This performance is shown in Table 1,2,3,4.

From Table 1, It shows that the clocked latches Basic 5T-TSPC and 5T-TSPC(MTCMOS) is designed to 0.18µm technology and VDD is 1.8v,The performance parameters of the latch is as, Number Of Transistors are 7 in 5T-TSPC(MTCMOS)and count of transistors are 5 in Basic 5T-TSPC.Even though the number of transistors and area is more in 5T-TSPC(MTCMOS) clocked latch the power consumption is reduced to 11.321µw compared to Basic 5T-TSPC clocked latch power is 19.56 µw.

From the Table 2, it clears that, the technology is scaled down to 0.12 µm but the supply voltage is high (1.8V), then the power consumption of clocked latches Basic 5T-TSPC is 14.120 µw and 5T-TSPC (MTCMOS) is 6.843 µw.

From the Table 3, it clears that, the technology is 0.18 µm but the supply voltage is 1.2V, then the power consumption of clocked latches Basic 5T-TSPC is 7.844 µw and 5T-TSPC (MTCMOS) is 4.286 µw.

From the Table 4,it clears that, the technology is scaled down to 0.12 µm but the supply voltage is also reduced (1.2V),then the power consumption of clocked latches Basic 5T-TSPC is 4.749 µw and 5T-TSPC(MTCMOS)is 2.340 µw.

5T-TSPC (MTCMOS) clocked latch having less power compared to Basic 5T-TSPC.

TABLE 1: Tech: 0.18µm VDD: 1.8V

Types Of Clocked Latches	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (μm^2)
Basic 5T-TSPC	5	1	Single	19.56	396
5T-TSPC (MTCMOS)	7	1	Single	11.321	576

TABLE 2: Tech: 0.12µm VDD: 1.8V

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Types Of Clocked Latches	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (µm²)
Basic 5T-TSPC	5	1	Single	14.120	144
5T-TSPC (MTCMOS)	7	1	Single	6.843	208

TABLE 3: Tech: 0.18µm VDD: 1.2V

Types Of Clocked Latches	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (µm²)
Basic 5T-TSPC	5	1	Single	7.844	396
5T-TSPC (MTCMOS)	7	1	Single	4.286	576

TABLE 4: Tech: 0.12µm VDD: 1.2V

Types Of Clocked Latches	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (µm²)
Basic 5T-TSPC	5	1	Single	4.749	144
5T-TSPC (MTCMOS)	7	1	Single	2.360	208

BILBO Design

The BILBO (Built-In-Logic-Block-Observer) has row of clocked latches. The clocked latch is D clocked latch. This section describes the design Of BILBO by using Basic 5T-TSPC clocked latch and by using 5T-TSPC (MTCMOS) clocked latch.

BILBO by using Basic 5T-TSPC Clocked latch

This section describes the BILBO (Built-In-Logic-Block-Observer) is designed by using Basic 5T-TSPC clocked latch. The general block diagram of BILBO is shown in Fig 2.In that Fig We replaced Basic 5T-TSPC clocked latch to D clocked latch. The schematic of BILBO by using Basic 5T-TSPC clocked latch is shown in Fig 5.

When B1&B2=1, Sin=0, x1, x2, x3=1, the output becomes zero. The clocked latches are reset. When B1&B2=1, Sin=1, x1, x2, x3=0, the clocked latches are reset. The BILBO is worked in Mode1.

When B1=1, B2=1 and x1, x2, x3=0, But Sin=1, the output becomes one. Because in latch the input is produced as same in output. When B1=1,B2=0,Sin=0,The clocked latch output becomes zero, the first clocked latch output is shifted to next.WhenB1=0,B2=0 and Sin=0, The BILBO is converted into an MISR(Multi Input Signature Register).

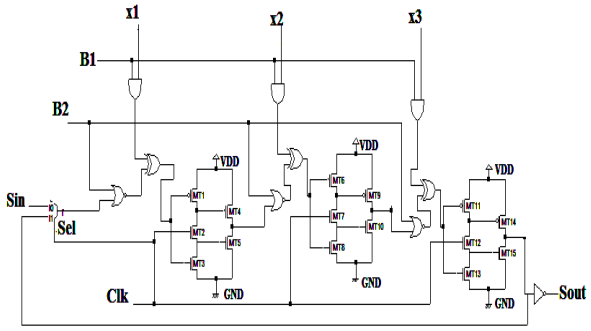

Fig 5: Schematic of BILBO by using 5T-TSPC Clocked Latch

BILBO by using 5T-TSPC (MTCMOS) Clocked latch

The proposed BILBO is designed by using 5T-TSPC (MTCMOS) clocked latch. The MTCMOS is introduced for reducing the power consumption. The MTCMOS technique is implemented by sleep transistors.

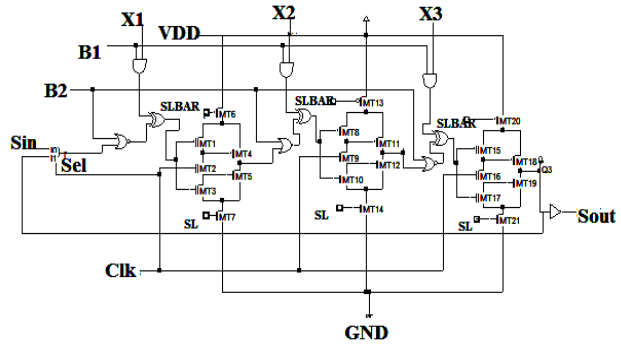

Fig 6: Schematic of BILBO by using 5T-TSPC (MTCOMS) Clocked Latch

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The same operation of designed BILBO by using Basic 5T-TSPC clocked latch is performed by this designed BILBO by using 5T-TSPC (MTCMOS) clocked latch. The performance of both BILBO is analyzed in terms of Number of Transistors (NT), Number Of clocked Transistors (NC), Power (P), and Area (A) .The performance parameter of BILBO is shown in Table 5.6,7,8.

TABLE 5: Tech: 0.18µm VDD: 1.8V

Types Of BILBO	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (μm^2)
BILBO by using Basic 5T-TSPC	17	3	Single	167.0	2968
BILBO by using 5T-TSPC (MTCMOS)	23	3	Single	93.786	4340

TABLE 6: Tech: 0.12µm VDD: 1.8V

Types Of BILBO	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (μm^2)
BILBO by using Basic 5T-TSPC	17	3	Single	89.429	840
BILBO by using 5T-TSPC (MTCMOS)	23	3	Single	237.0	1241

TABLE 7: Tech: 0.18µm VDD: 1.2V

Types Of BILBO	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (μm^2)
BILBO by using Basic 5T-TSPC	17	3	Single	55.323	2968
BILBO by using 5T-TSPC (MTCMOS)	23	3	Single	18.940	4340

TABLE8: Tech: 0.12µm VDD: 1.2V

Types Of BILBO	No. of Transistors (NT)	No. of Clocked Transistors (NC)	Triggering	Power (P) (µW)	Area (A) (μm^2)
BILBO by using Basic 5T-TSPC	17	3	Single	26.878	840
BILBO by using 5T-TSPC (MTCMOS)	23	3	Single	17.009	1241

From the table 5,6,7,8,It clears that the power consumption is less in 0.12µm technology and supply voltage is 1.2v.The power consumption of BILBO by using 5T-TSPC(MTCMOS) clocked latch is reduced to 17.00µw.This power is less compared to BILBO is designed by using Basic 5T-TSPC clocked latch.i.e(26.878µw).Table 5 describes the BILBO is applied to 0.18µm technology and VDD is 1.8v.The power consumption of BILBO is more (0.167mw) for designed BILBO by using Basic 5T-TSPC clocked latch and this power is reduced to 93.786µw in BILBO is designed by using 5T-TSPC(MTCMOS)clocked latch.

Simulation Results and Discussion

In this section, the clocked latches Basic 5T-TSPC, 5T-TSPC (MTCMOS) and BILBO by using Basic 5T-TSPC, BILBO by using 5T-TSPC (MTCMOS) circuit's performance is analyzed from the simulation results.

The simulation results are obtained by using DSCH tool and Microwind is a user friendly EDA tool for designing the chip. It is a logic editor and

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simulator for hierarchical design of chip. The clocked latches Basic 5T-TSPC, 5T-TSPC (MTCMOS) and the BILBO by using Basic 5T-TSPC, BILBO by using 5T-TSPC (MTCMOS) circuit layout is obtained. The layout shows the interconnection between the polysilicon and diffusion are made through contacts. From the layout the area occupation of circuit is calculated. The simulation result shows power consumption of each designed circuit. With the feature size is scaled down, the power consumption of 5T-TSPC (MTCMOS) is less (2.360µw) compared to Basic 5T-TSPC clocked latch (4.749µw) and the power consumption of designed BILBO by using 5T-TSPC (MTCMOS) clocked latch is less (17.009µw) compared to BILBO by using Basic 5T-TSPC clocked latch (26.878µw).The MTCMOS technique is used to reduce leakage power. The number of transistors and clocked transistors are reduced in the designed clocked latches and BILBO compared to conventional clocked latches and BILBO. That is the reason for power reduction in our proposed clocked latches and BILBO circuits. The simulation results of BILBO by using Basic 5T-TSPC clocked latch and BILBO by using 5T-TSPC(MTCMOS) is shown in Fig 7,8,9,10,11,12.

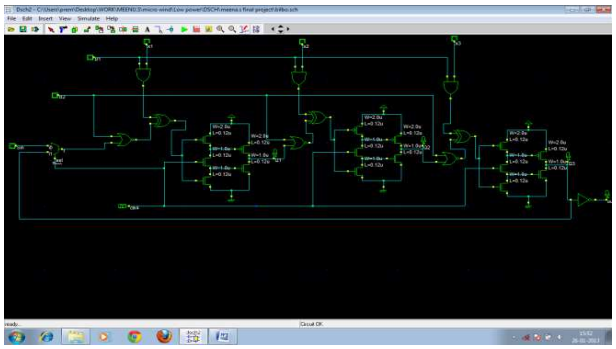

Fig: 7 Schematic of BILBO by using Basic Clocked latch

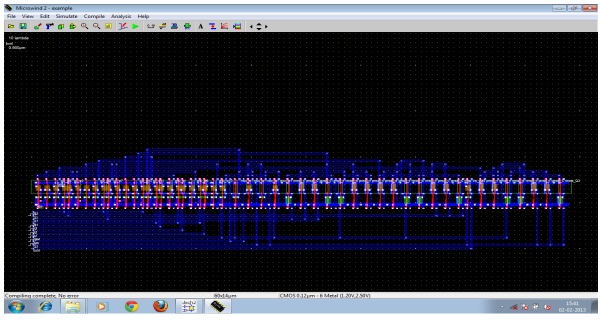

Fig: 8 Layout of BILBO by using basic 5T-TSPC Clocked latch

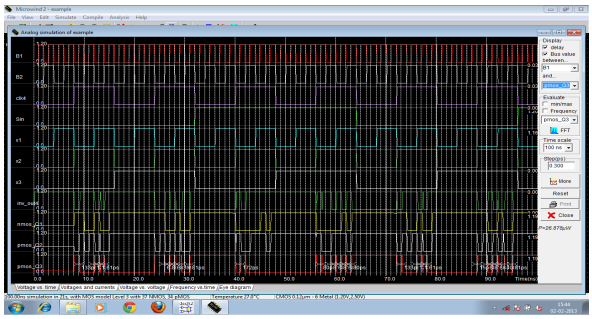

Fig: 9 Simulation Output of BILBO by using Basic 5T-TSPC clocked latch

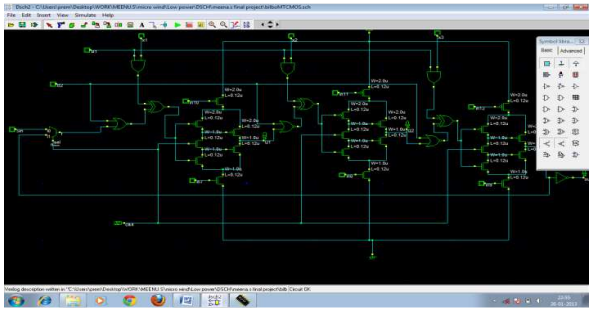

Fig10: Schematic of BILBO by using 5T-TSPC (MTCMOS) clocked latch

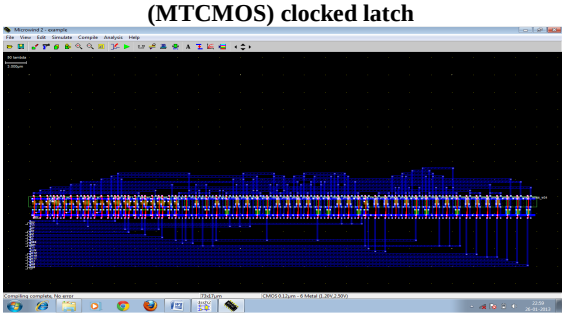

Fig11: Layout of BILBO by using 5T-TSPC (MTCMOS) clocked latch

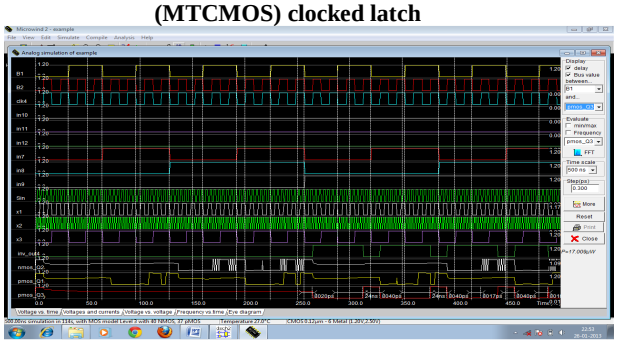

Fig12: Simulation Output of BILBO by using 5T-TSPC (MTCMOS) clocked latch

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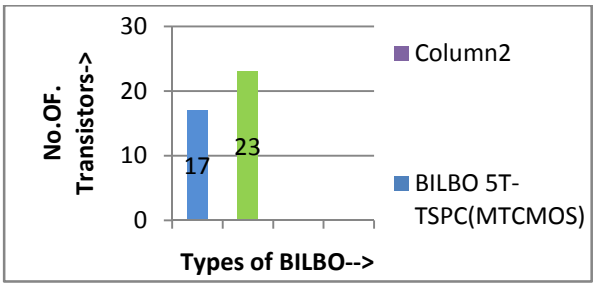

Fig 13: Types of BILBO Vs No. Of Transistors

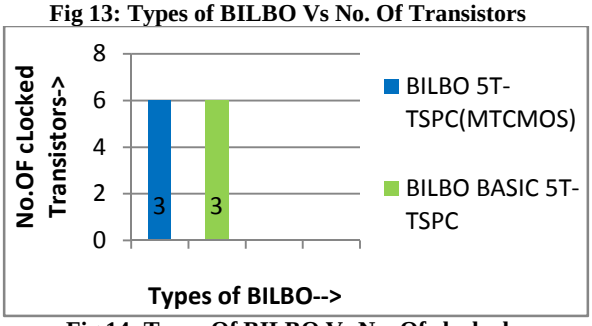

Fig 14: Types Of BILBO Vs No. Of clocked Transistors

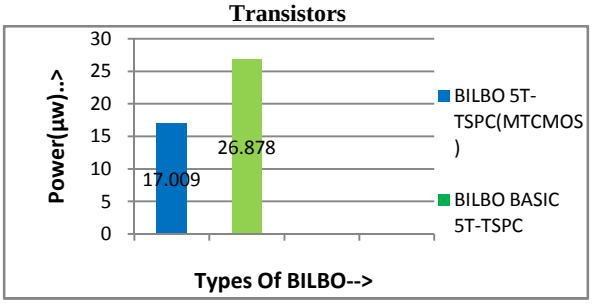

Fig: 15 Types of BILBO Vs Power consumption

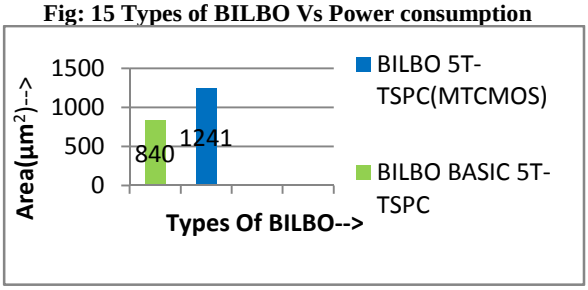

Fig: 16 Types of BILBO Vs Area

Conclusion

From the simulation results it is concluded that the 5T-TSPC (MTCMOS) clocked latch consumes less power than the Basic 5T-TSPC clocked latch. By applying MTCMOS technology 51% of power is reduced in the 5T-TSPC (MTCMOS) clocked latch. The design of BILBO using 5T-TSPC (MTCMOS) clocked latch with supply voltage VDD 1.2V**,**Technology,0.12µm consumes less power(17.009µw) than that of using BILBO using Basic 5T-TSPC clocked latch(26.876µw).

The Proposed BILBO by using 5T-TSPC (MTCMOS) clocked latch outperforms by about 34% of power reduction.

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